

MPEG-2 DeMUX, HDTV Decoder, Display Processor and Microcontroller Single Chip

HiPEG+

Overview

Mikrom's HiPEG+ is a single chip MPEG-2 HDTV video decoder and display processor which also includes the transport stream demultiplexer and a 32bit RISC CPU.

This offers a very cost effective high integrated solution for Settop-Box applications. DVB and all 18 ATSC formats are supported making this chip applicable worldwide.

MPEG decoding, display processing and transport demultiplexing are implemented in hardware. The display processor supports a broad range of resolutions, formats and modes for various displays.

The on-chip RISC CPU, operating at 54 MHz, is fully available for customer application software. An optional external system CPU can control all functions too.

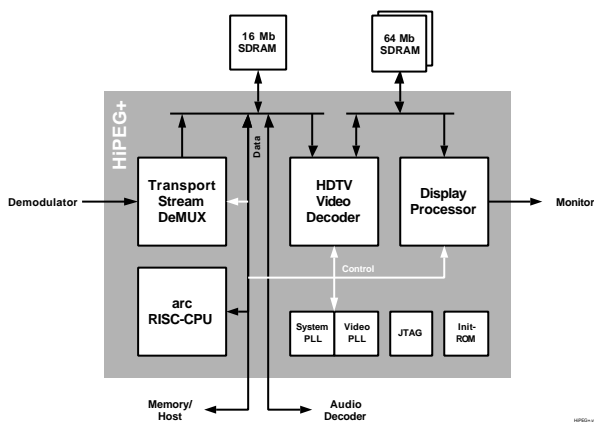
In addition the chip provides advanced features like up/downscaling (HDTV <-> TV!), letterbox format conversion up to Y_CR_CB/RGB conversion.

Features

- Transport Demultiplexer DeMUX
 - Demultiplexing of MPEG-2 Systems, ISO/IEC 13818-1
 - ATSC/DVB-System Information capture
 - Private data capture
 - Flexible Audio/Video synchronization (Lips Synchronicity)
 - Dedicated hardware for PID/section filtering
 - Individual filter allocation for each transport stream (PID)
 - Supports for 32 PIDs:
 - 1 PID video, 1 PID audio, 1 PID teletext buffer
 - 29 PIDs for section data
 - Multi mode input for coded data: TS, Video-PES, Video-ES
 - DVB compliant SPI interface
 - 160 Mbps max. input data rate
- Up to 15 bytes after section length can be compared
- Dedicated hardware for clock recovery (PWM generation)
- Video Decoder
 - Decoding of MPEG-2 Video MP@HL, ISO/IEC 13818-2
 - Decodes images up to 1080i 60 Hz or 1080p 30 Hz
 - Support includes all 18 ATSC formats
 - Error concealment based on temporal processing
 - 4 Frame architecture utilising various pulldown applications
- Display Processor
 - Digital SDTV/HDTV output supports various PAL/NTSC and HDTV Standards (ITU-R BT.601/656, ITU-R BT.709/1120, SMPTE 274 M)
 - Up/Downconversion (Zoom), factor 4, horizontal 8 tap, vertical 2 tap, h/v independent for Letterbox,...
 - Aspect Ratio Conversion
 - Chrominance upsampling: 4:2:0 -> 4:2:2 -> 4:4:4
 - Automatic frame rate conversion, 3/2 Pull-Down
 - Horizontal, vertical pan&scan
 - Interlace/Progressive Conversion (LD, FM)
 - 8b Y_CR_CB- or RGB-output
 - Free programmable RGB coefficients
 - R, G, B, HSync, VSync, Blank, Parity; direct connectable to DAC or PDP
 - Video clock in- and output
- Audio Decoder Interface
 - ES output, Master/Slave mode
 - Various digital audio output modes (I2S, frameless)
- RISC CPU integrated (32bit)
 - 1 kB instruction cache
 - 54 MHz clock, 54 Mips
 - Debug interface
 - CPU Interface
 - Host/Standalone mode
 - Host: RISC disabled, direct connection of various CPUs like SparcLite, MC68k, PowerPC, FR30 or PCI-Bridge

- Standalone: RISC enabled, direct connection of RAM, SDRAM or FLASH
- System clock 27 MHz
- On-chip video APLL for 13.5 - 81 MHz
- Timer, Infrared-receiver
- Configurable SDRAM sequencers
- 0.25 micron CMOS technology
- Power < 2 W
- Voltage 3.3 V/2.5 V
- Package PBGA 352
- Boundary Scan, IEEE 1449.1

Block Diagram



Applications

Basing on HiPEG, one of world's first high integrated, hardware proven HDTV decoder, HiPEG+ is enhanced and optimized for consumer and commercial applications. Typical online applications are Set-Top Boxes STB and Integrated Receiver Decoder IRD.

To ease integration into offline applications like HD/DVD-based playback systems HiPEG+ provides additional functions and interface signals: Beyond TS HiPEG+ also accepts PES/ES data with an automatic start-decoding mechanism; a vbv_buffer fillness control signal is provided for automatic request of PES/ES-data from external HD/DVD.

The clock system is flexible usable for internal or external video clock generation (Genlocking). Auxiliary video clock outputs simplify connection to video postprocessing devices like RAMDAC.

The display processor output can be synchronized from external via a simple 2-wire handshaking interface (e.g. cross-connected with another HiPEG+) to synchronize the output of video frames. Together with external video clock input this feature is usefull wherever synchronized HDTV outputs are needed. Application examples are 3D, large screen projection, video walls.

In case of a powerfull external system processor the internal RISC-CPU is turned off (Host mode) and the µP interface is used to access the HiPEG+ registers from external. The almost generic µP interface supports a wide range of system processor architectures, especially FR30, MC68k, SparLite, PowerPC. Even the glueless connection e.g. to a PCI-Bridge in PC-based applications is aided.

For standalone applications, where no external system processor is available (Standalone mode), the capabilities of the internal 32bit RISC-CPU can be used for initialisation, control and interfacing of internal or external devices. The memory system of the RISC-CPU directly supports SRAM/SDRAM/FLASH and is connected via the µP interface. Free address space allows external chip-select generation to connect additional devices.

A full featured commercial C/C++ development tool system including compiler/assembler/linker/debugger on different platforms (NT/9x, SunOS/Solaris) is available from MetaWare Inc. (www.metaware.com).

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